forming one or more recesses extending from the second surface of the substrate into interior portions of the semiconductor substrate; and

forming a resistivity-lowering body in one or more of the recesses, the resistivity-lowering bodies comprising a material having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate.

55.(amended) A method according to Claim 52 further comprising forming a barrier layer lining at least one recess.

56.(amended) A method according to Claim 52 wherein forming the resistivity-lowering body comprises forming said body using an electrical conductor having an electrical resistivity less than about 10^{-4} Ω•cm.

57.(amended) A method according to Claim 52 wherein forming the recesses and associated resistivity-lowering body comprises forming the recesses and the assoicated resistivity lowering bodies to define a proportion of the semiconductor substrate area adjacent the at least one device active region no less than than about 0.4 percent.

58.(amended) A method according to Claim 52 wherein forming the recesses and associated resistivity-lowering body comprises forming the recesses and the associated resistivity lowering bodies to extend into the semiconductor substrate a distance greater than about 25 percent of a thickness of the semiconductor substrate.

60.(amended) A method according to Claim 59 wherein forming the array of recesses and associated resistivity-lowering bodies comprises are arranged in a grid pattern.

65.(amended) A method for making a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method comprising:

in a first surface, forming one or more well regions comprising dopants of one polarity;

in the first surface and in said body regions, forming source regions of dopants of an opposite polarity, the source regions laterally spaced from each other;

forming gate regions between the laterally spaced source regions;

in a second surface opposite the first surface, forming a layer of dopants;

removing material from the second surface to reduce the thickness of said substrate;

and forming one or more resistivity-lowering bodies extending from the second surface of the substrate into interior portions of the semiconductor substrate, the resistivity-lowering bodies comprising a material different than the semiconductor substrate and having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate.

67.(amended) A method according to Claim 65 wherein the at least one resistivity-lowering body comprises an electrical conductor having an electrical resistivity less than about 10^{-4} Ω•cm.

68.(amended) A method according to Claim 65 wherein the resistivity-lowering body comprises forming the resistivity-lowering body to define a proportion of the semiconductor substrate area adjacent the at least one device active region not less than than about 0.4 percent.

69.(amended) A method according to Claim 65 wherein the resistivity-lowering body extends into the semiconductor substrate a distance greater than about 25 percent of a thickness of the semiconductor substrate.

71.(amended) A method according to Claim 70 wherein the array of resistivity-lowering bodies comprises a grid pattern.

REMARKS

This amendment is submitted in response to the office action mailed August